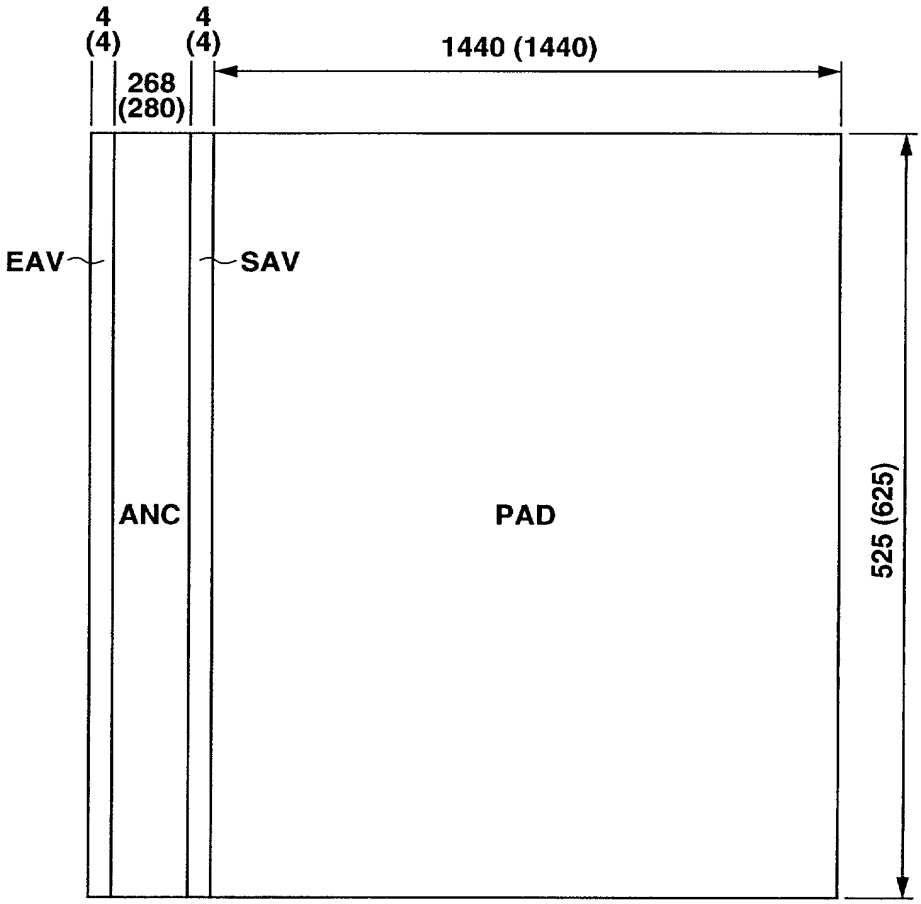


FIG.1

FIG.2A

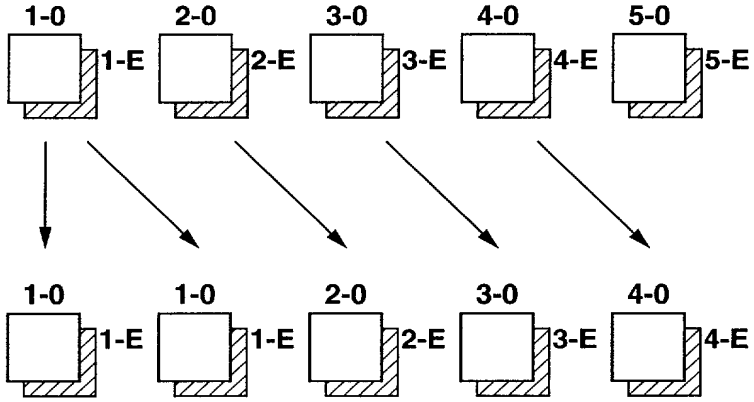
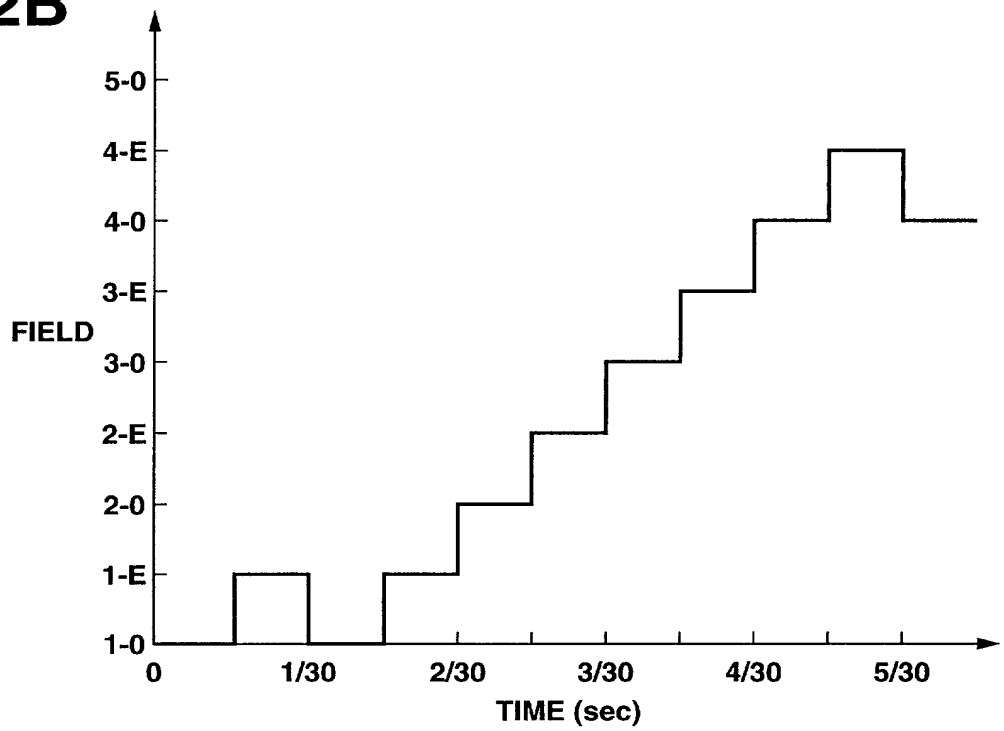

1-0
2-0
3-0
4-0
5-0
1-E
2-E
3-E
4-E
5-E
1-0
1-0
2-0
3-0
4-0
1-E
1-E
2-E
3-E
4-E

FIG.2B


FIELD
5-0
4-E
4-0
3-E
3-0
2-E
2-0
1-E
1-0
0
1/30
2/30
3/30
4/30
5/30
TIME (sec)

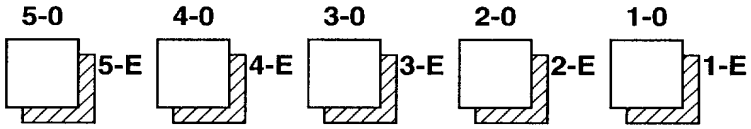


FIG.3A

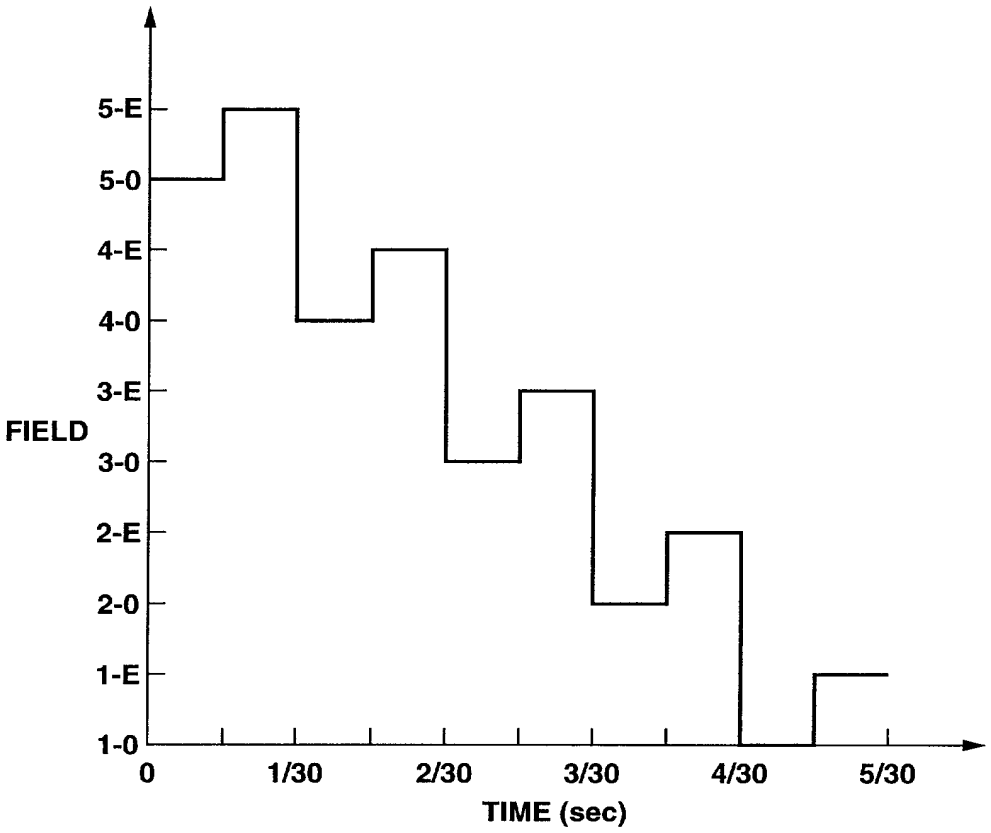


FIG.3B

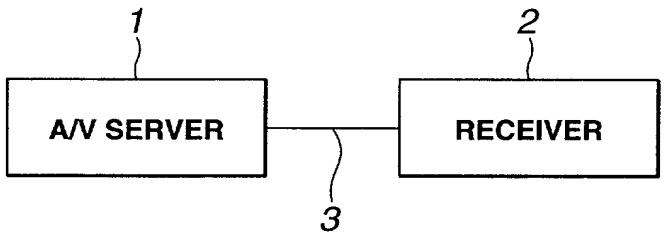


FIG.4

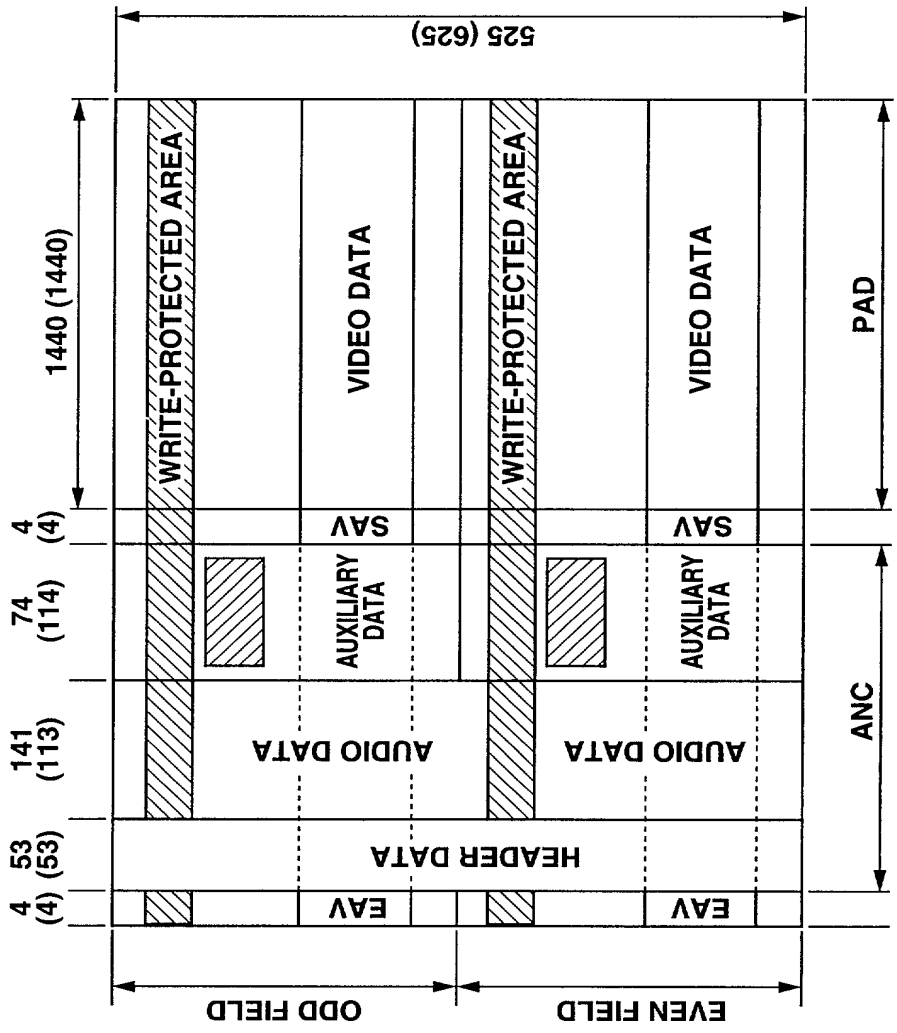

525 (625)
1440 (1440)
WRITE-PROTECTED AREA
VIDEO DATA
WRITE-PROTECTED AREA
VIDEO DATA
PAD
4 (4)
SAV
SAV
74 (114)
AUXILIARY DATA
AUXILIARY DATA
141 (113)
AUDIO DATA
AUDIO DATA
ANC
53 (53)
HEADER DATA
4 (4)
EAV
EAV
ODD FIELD
EVEN FIELD

FIG.5

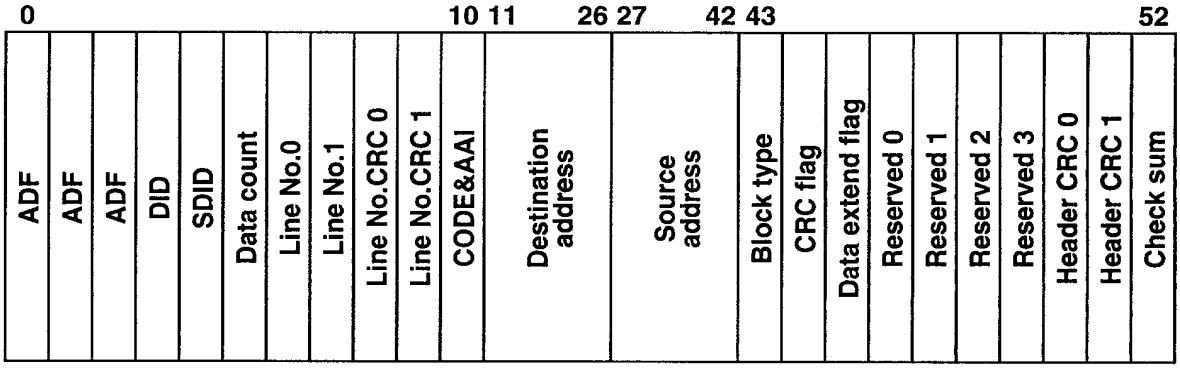

0
10 11
26 27
42 43
52
ADF
ADF
ADF
DID
SDID
Data count
Line No.0
Line No.1
Line No.CRC 0
Line No.CRC 1
CODE&AAI
Destination address
Source address
Block type
CRC flag
Data extend flag
Reserved 0
Reserved 1
Reserved 2
Reserved 3
Header CRC 0
Header CRC 1
Check sum

FIG.6

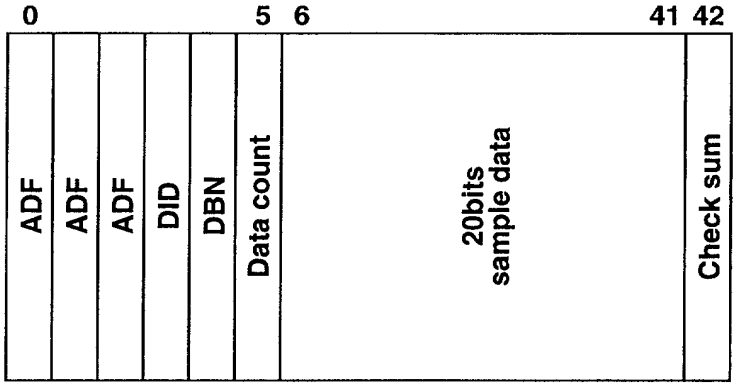

0
5
6
41
42
ADF
ADF
ADF
DID
DBN
Data count
20bits
sample data
Check sum

FIG.7A

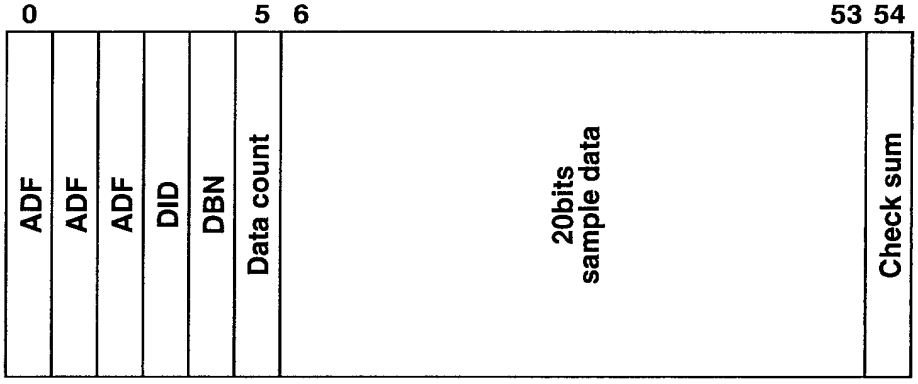

0
5
6
53
54
ADF
ADF
ADF
DID
DBN
Data count
20bits
sample data
Check sum

FIG.7B

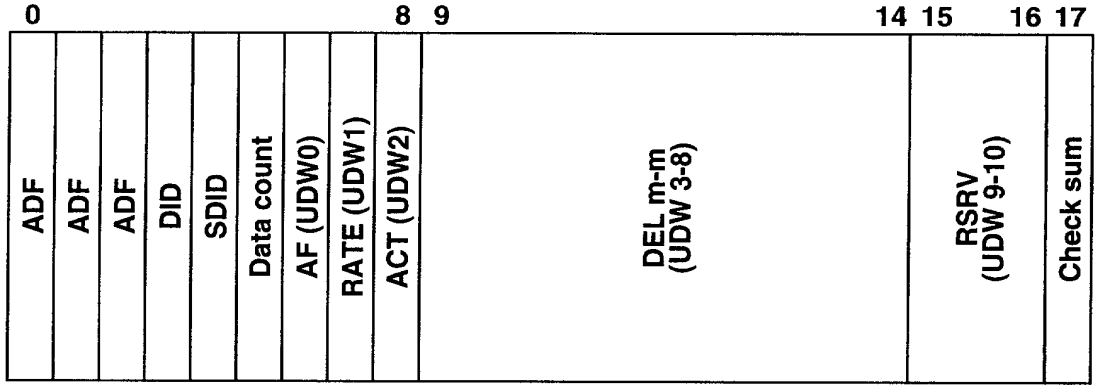

0
8
9
14
15
16
17
ADF
ADF
ADF
DID
SDID
Data count
AF (UDW0)
RATE (UDW1)
ACT (UDW2)
DEL m-m
(UDW 3-8)
RSRV
(UDW 9-10)
Check sum

FIG.8

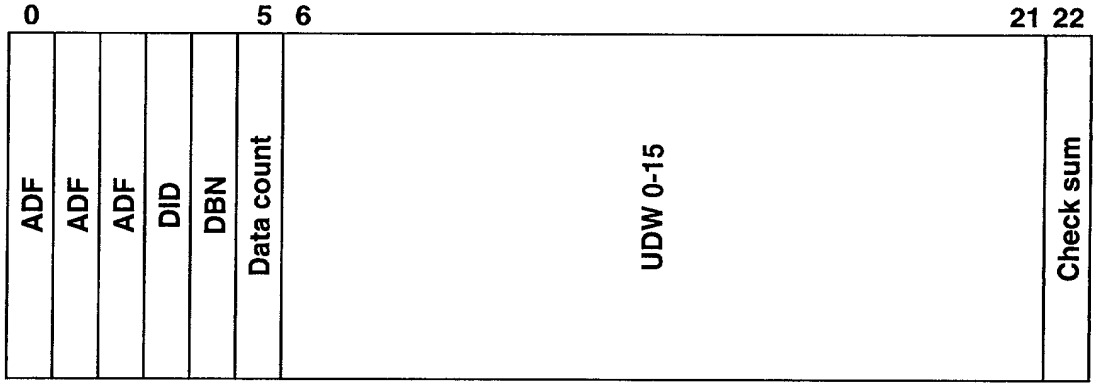

0
5
6
21
22
ADF
ADF
ADF
DID
DBN
Data count
UDW 0-15
Check sum

FIG.9

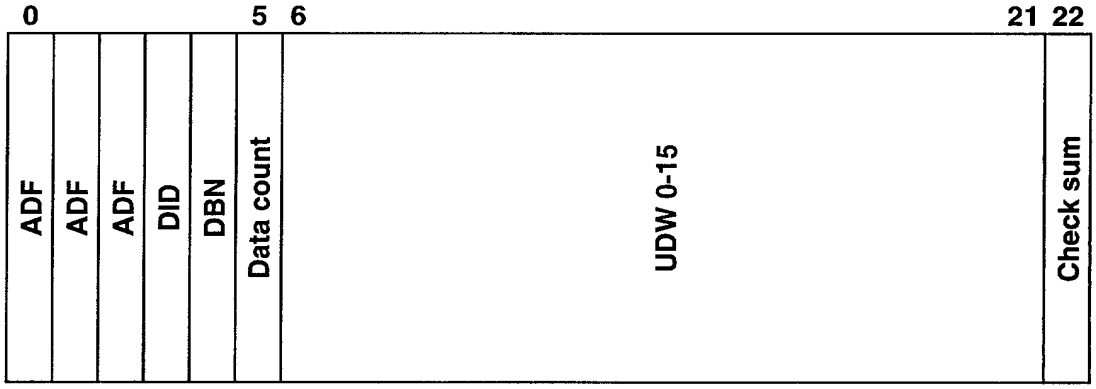

0
5
6
21
22
ADF
ADF
ADF
DID
DBN
Data count
UDW 0-15
Check sum

FIG.10

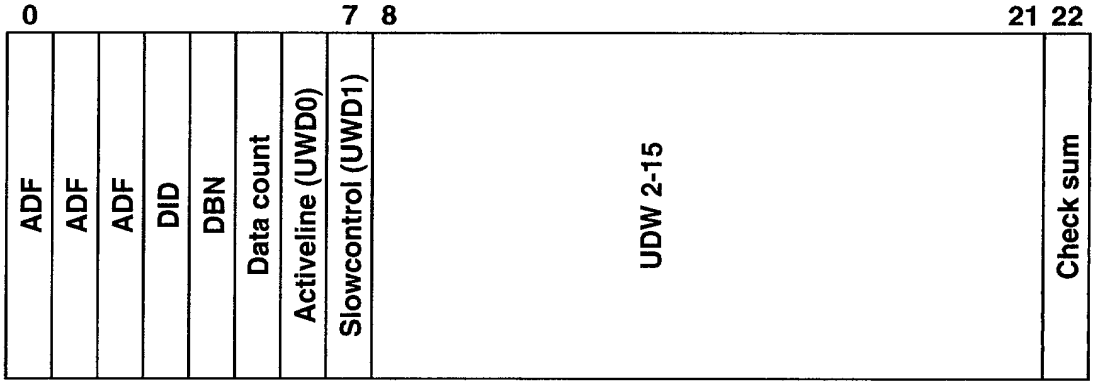

0
7
8
21
22
ADF
ADF
ADF
DID
DBN
Data count
Activeline (UWD0)
Slowcontrol (UWD1)
UDW 2-15
Check sum

FIG.11

BIT	
7	Reserved
6	Reserved
5	Reserved
4	Contents information
3	Combination of the memory address
2	
1	
0	

FIG.12

FIG.13A

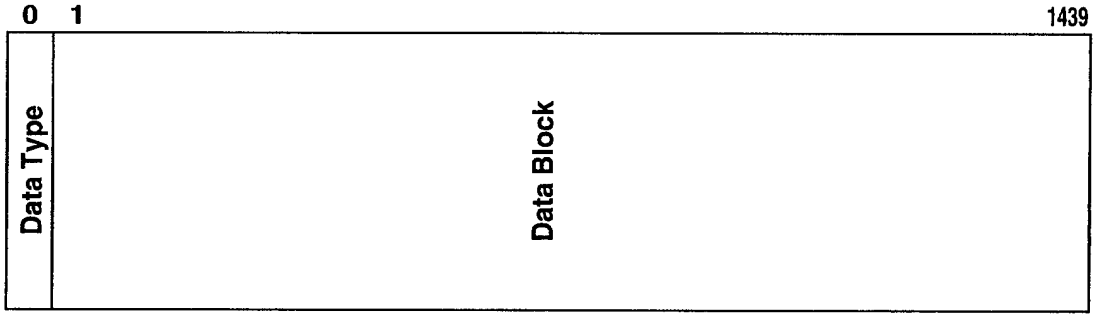
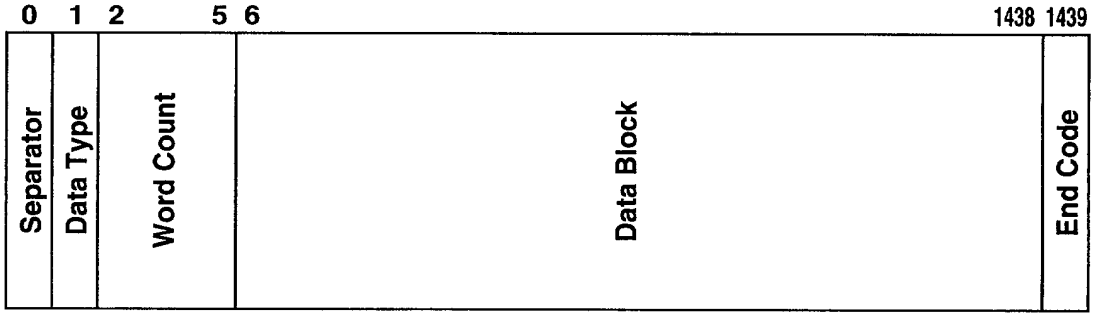


FIG.13B



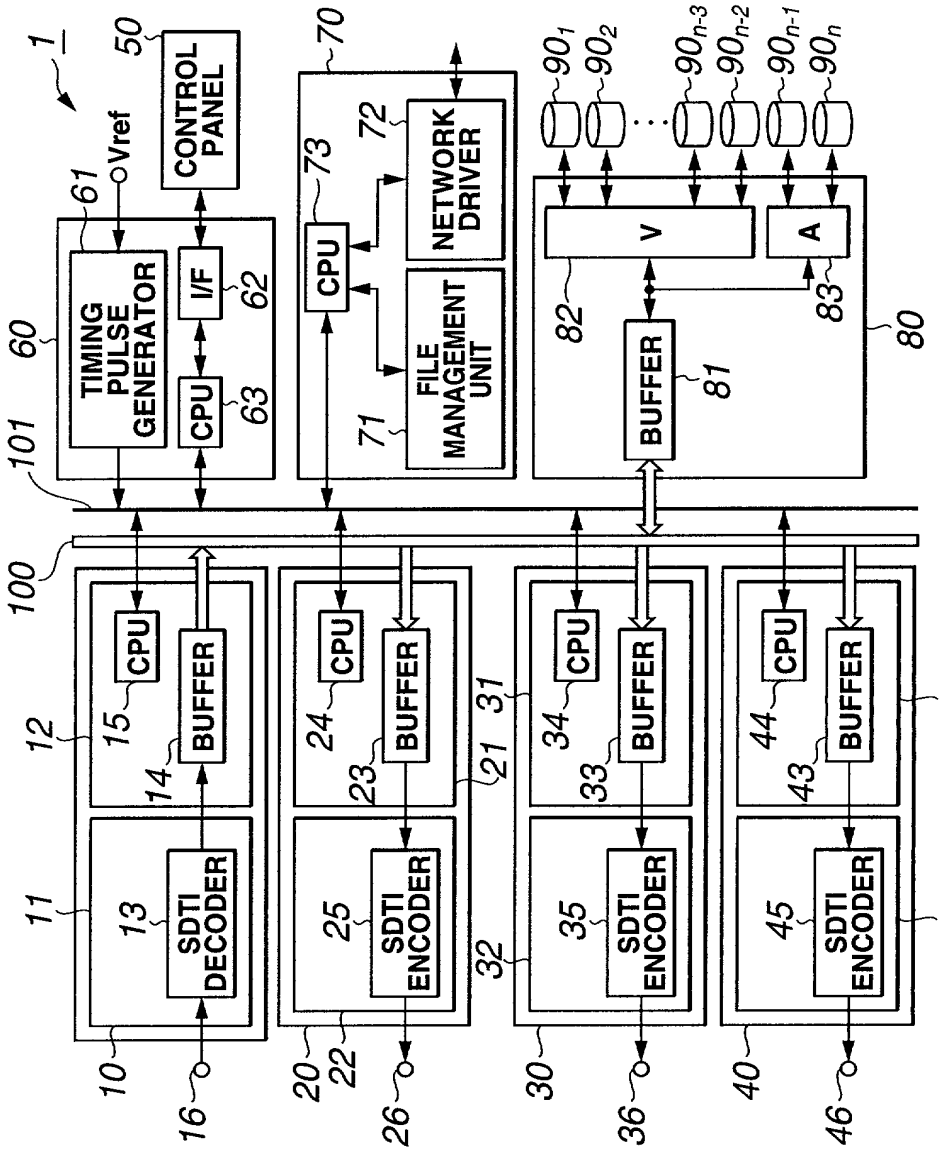

1
50
CONTROL PANEL
Vref
61
60
TIMING PULSE GENERATOR
I/F
62
CPU
63
101
70
73
CPU
72
NETWORK DRIVER
71
FILE MANAGEMENT UNIT
90_1
90_2
90_{n-3}
90_{n-2}
90_{n-1}
90_n
V
A
82
83
80
BUFFER
81
100
12
15
CPU
BUFFER
14
11
13
SDTI DECODER
10
16
24
CPU
BUFFER
23
21
31
25
SDTI ENCODER
32
20
22
26
34
CPU
BUFFER
33
35
SDTI ENCODER
30
36
44
CPU
BUFFER
43
41
45
SDTI ENCODER
42
40
46

FIG.14

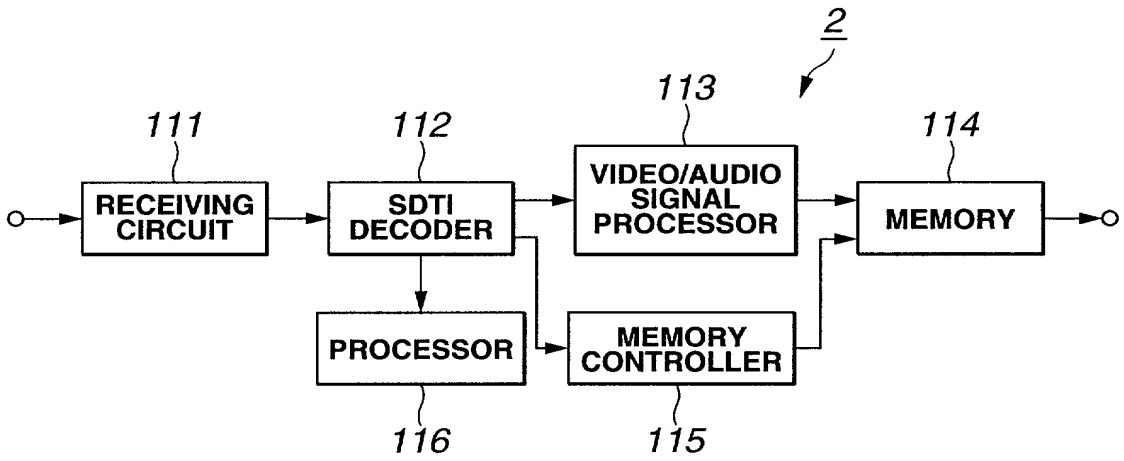

2
111
112
113
114
RECEIVING CIRCUIT
SDTI DECODER
VIDEO/AUDIO SIGNAL PROCESSOR
MEMORY
PROCESSOR
MEMORY CONTROLLER
116
115

FIG.15

FIG.16A

FIG.16B

FIG.16C

FIG.17A

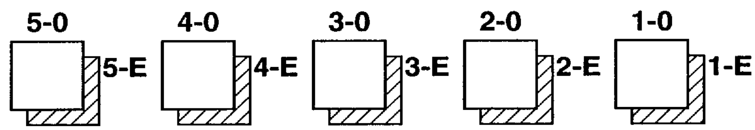


FIG.17B

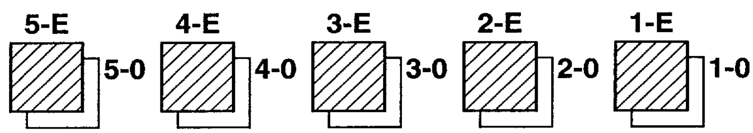


FIG.17C

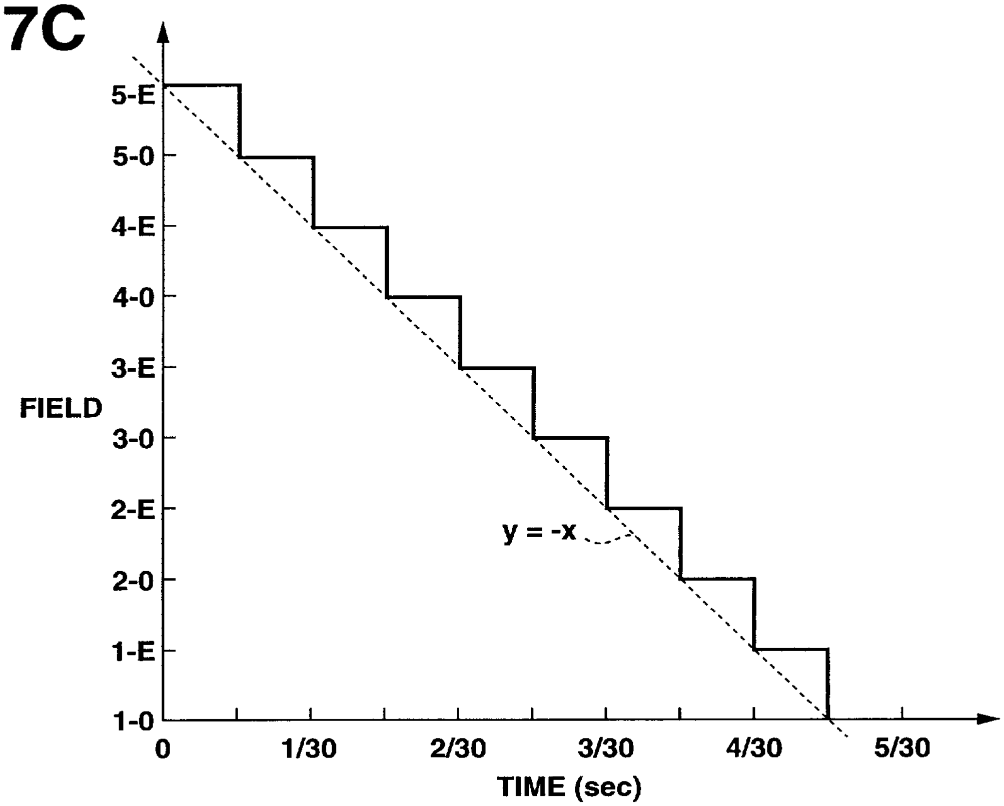


FIG.18A

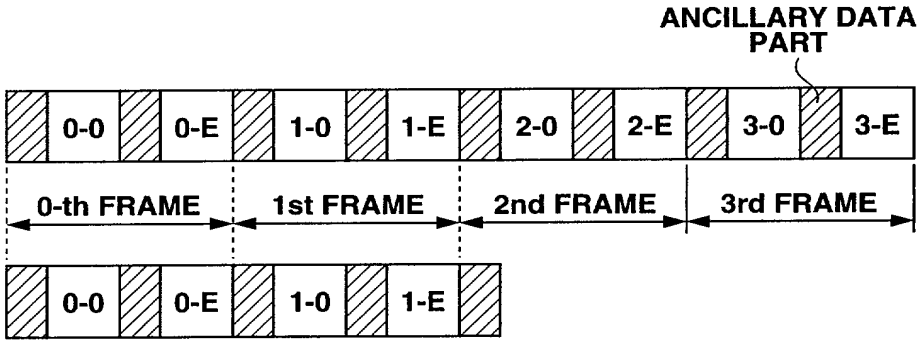


FIG.18B

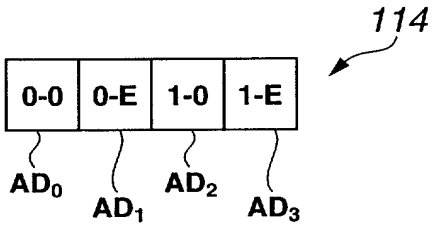


FIG.18C

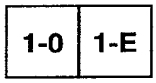


FIG.18D

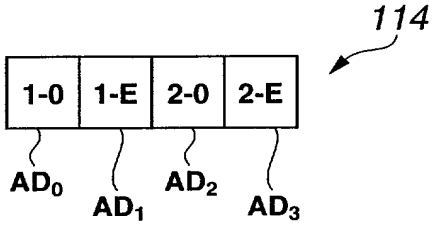


FIG.19A

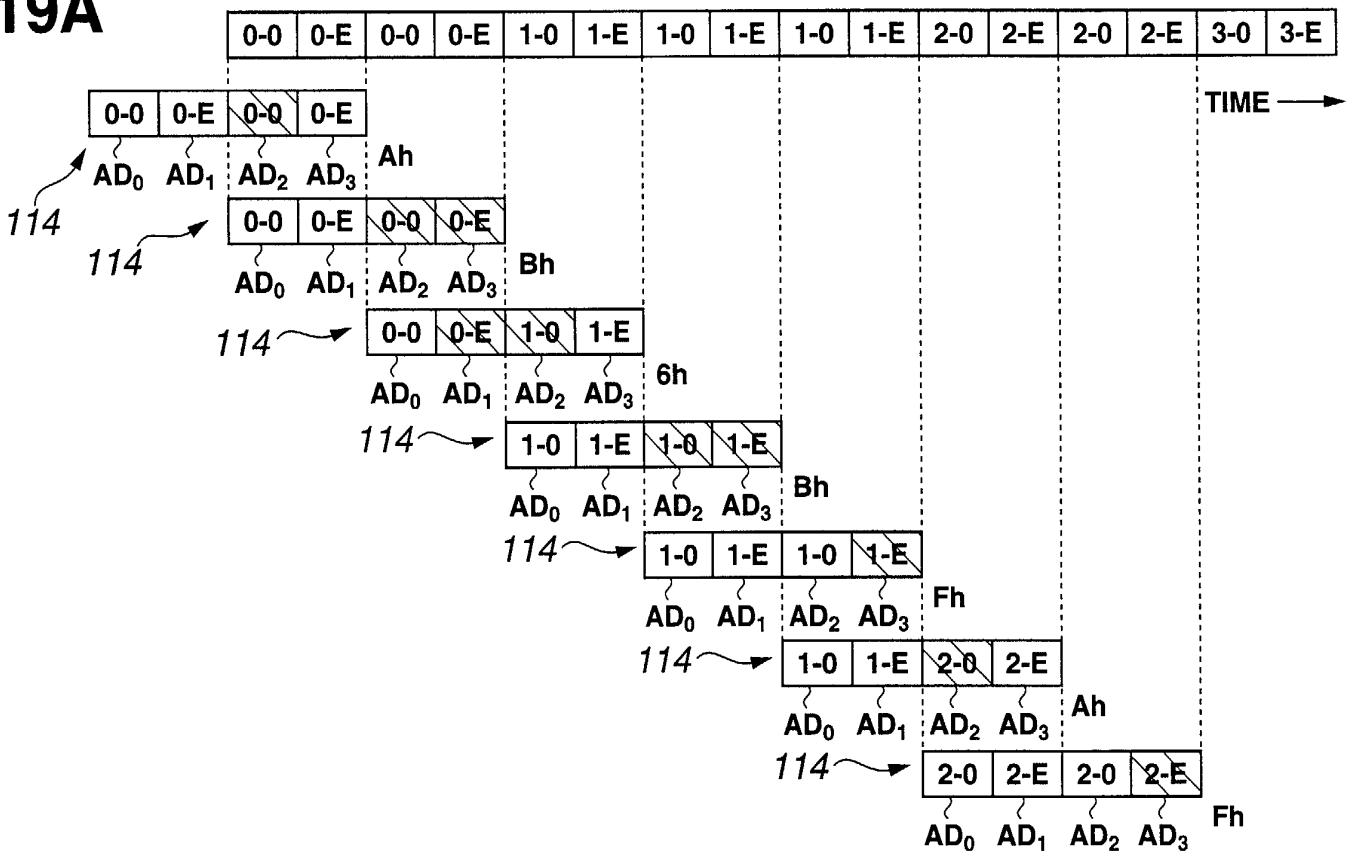


FIG.19B